



## ANSYS Expands Its Solutions for TSMC Advanced Package Technology to Meet Growing Performance, Reliability and Power Demands

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*TSMC and ANSYS enable multi-die analysis in advanced packaging technologies*

**PITTSBURGH, April 30, 2018** – [TSMC](#) validates [ANSYS® RedHawk™](#), ANSYS® RedHawk-CTATM and ANSYS® CSMTM for TSMC Wafer on Wafer (WoW) and Chip on Wafer on Substrate (CoWoS®) advanced packaging technologies. The solutions include die and package co-simulation and co-analysis for extraction, power and signal integrity analysis, power and signal electromigration analysis and thermal analysis. CoWoS and WoW technologies enable smaller package size through multiple dies integration.

"Advanced packaging technologies will be the key driver for achieving extreme performance, high-system bandwidth and low power in leading-edge high-performance computing (HPC), cloud computing and automotive electronics systems," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "The solution enablement with ANSYS supports customers performing advanced multi-die simulations to achieve their desired performance and reliability goals."

"Through exploration, prototyping and signoff, ANSYS' industry-leading solutions can be used across the entire design spectrum, from chip to package to system," said John Lee, general manager at ANSYS. "Close collaboration and partnership with TSMC ensures customers can design next-generation semiconductor chips with confidence."

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### **Contact**

#### **Media**

Mary Kate Joyce  
724.820.4368  
[marykate.joyce@ansys.com](mailto:marykate.joyce@ansys.com)

#### **Investors**

Annette Arribas, CTP  
724.820.3700  
[annette.arribas@ansys.com](mailto:annette.arribas@ansys.com)